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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,017	04/24/2006	Eiji Takaike	CU-4798 RJS	7524
26530 7590 06/16/2009 LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1600 CHICAGO, IL 60604				
EXAMINER				
GREEN, TELY D				
ART UNIT		PAPER NUMBER		
2822				
MAIL DATE		DELIVERY MODE		
06/16/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/577,017

Applicant(s)

TAKAIKE, EIJI

Examiner

TELLY D. GREEN

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 April 2009.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-12, 16 and 17 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-3, 5-12, 16 and 17 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SI-08)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments filed April 6, 2009 have been fully considered but they are not persuasive. Applicant argues on pages 6-8 that Yamane in view Anderson teach away from each other. The examiner respectfully disagrees. The applicant chooses to argue on pages 7 and 8 about the **process** that would produce an electronic element and an interposer made of silicon in regards to combination of Yamane and Anderson. Examiner would like note that the applicant has chosen device claims for prosecution. The combination of Yamane and Anderson discloses the structure of the claimed invention. As state below in the rejection, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the electronic element(s) or chip(s) and the interposer/interposer base of Yamane with Anderson's electronic element(s) or chip(s) and interposer/interposer base(s) made of silicon for the purpose of having the same thermal expansion coefficient. The examiner takes the position the rejection is proper.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1- 3, 5-11 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (Yamane) (**US Publication 2004/0070064 A1**) in view of Anderson et al. (**US Publication 2003/0038415 A1**).

In regards to claims **1-3, 5 – 11, 16**, Yamane discloses (**Figs. 20K-20N, 210, 231-24M, 50**) an electronic element (**item 20**); and an interposer (**items 50/72, 74, 72 plus 74, 48 plus 14 plus 50/72 plus 74**) including an interposer base (**item 50, 72, 74 or 50/72 plus 74**) to which the electronic element is joined, and a plurality of post electrodes (**items 18, 23**) that are disposed inside one or more through holes (**portions where items 18 and 23 are formed**) formed in the interposer base and are connected to corresponding electrodes (**item 22**) of the electronic element; wherein a surface of the electronic element (**item 20**) and a surface of the interposer base (**bottom portion of item 50/72, 74 or 50/72 plus 74**) are integrated with each other by being brought into direct contact with each other, and the post electrodes (**item 23**) are formed directly on the corresponding electrodes of the electronic element, first and second insulating layer (**items 14, 24, Figs. 41**), a recess to accommodate electronic element (**Figs. 19I, 19J, 20K-20M**) a plurality of electronic elements (**items 20 and 30**) mounted to the interposer base (**Fig. 41**) and a sealing resin (**item 40, Fig.41**) encapsulating the electronic element is disposed on the interposer base, but does not specifically disclose wherein the electronic element and the interposer are made of silicon.

Anderson discloses the electronic element and the interposer base are made of silicon/same material (**paragraphs 22, 23**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of having a chip and an interposer/interposer base with approximately the same thermal expansion coefficient (**paragraph 23**).

Claim **12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (Yamane) (**US Publication 2004/0070064 A1**) in view of Anderson et al. (Anderson) (**US Publication 2003/0038415 A1**) as applied to claims **1-3, 5-11 and 16** above, and further in view of Terui (**US Publication 2004/0150104 A1**).

In regards to claim 12, Yamane as modified by Anderson does not specifically disclose wherein the electronic element is a passive element.

Terui discloses (**Figs. 4, 6, 12, 16**) wherein the electronic element is a passive element (**paragraph 76**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of regulating electrical characteristics (**paragraph 19**).

Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (Yamane) (**US Publication 2004/0070064 A1**) in view of Anderson et al. (Anderson) (**US Publication 2003/0038415 A1**) as applied to claim 16 above, and further in view of Chakravorty et al. (Chakravorty) (**US Publication 2003/0185484 A1**).

In regards to claim 17, Yamane as modified by Anderson does not specifically disclose wherein the electronic element is an optical device; and the interposer is provided with an optical waveguide optically connected to the optical device.

Chakravorty discloses wherein the electronic element is an optical device; and the interposer is provided with an optical waveguide optically connected to the optical device

(Abstract, paragraphs 11-14).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings above for the purpose of optical and electrical functionality.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **TELLY D. GREEN** whose telephone number is (571)270-3204. The examiner can normally be reached on Monday thru Friday 7:30 AM - 5:00 PM EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art
Unit 2822

/Telly D Green/
Examiner, Art Unit 2822
June 11, 2009